DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 8 are also rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (USP 6,489,828).

With respect to claims 1, 7 and 8, Figure 3 of Wang et al. teaches a level shift circuit, which includes: first (MP2) and second (MP3) P-channel transistors; a high voltage power supply (VDDH); first (MN2) and second (MN3) N-channel transistors; complement input signals (216 and 217) and a resistance element (MN4) with the connections (including the limitation of "directly conencted") as recited in claim 1 and wherein the drain of the second N-channel transistor (MN3) servers as a first output terminal (OUT) to a high power supply voltage operating circuit.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uenishi et al. (USP 6,617,896) in view of Nojiri (US 2001/0013795 A1).

With respect to claims 1 and 8, Figure 11A of Uenishi et al. teaches a level shift circuit, which includes: first (Qp1) and second (Qp2) P-channel transistors; a high voltage power supply (VDD2); first (Qn1) and second (Qn2) N-channel transistors; complement input signals (104, 105); wherein the drain of the second N-channel transistor (Qn2) serves as a first output terminal (102) to a high-power supply operating circuit with the connections (including the limitation "directly connected") as recited in the claim. Figure 11A of Uenishi et al. does not teach the level shift circuit further comprises a resistance element connected between the output terminals of the level shifter circuit. However, Figure 8 of Nojiri teaches a level shifter including a resistance element (P5) connected between the outputs (W1, W2) of the level shifter circuit. Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the level shifter in Figure 11A of Uenishi et al. to include a resistance element (P5) as taught in Figure 8 of Nojiri to improve the speed of the level shifter circuitry. Thus, this modification meets all the limitations of claims and 8 including the limitation that the level shifter including a resistance element (P5, Figure 8 of Nojiri) connecting

between the drains of the first N-channel transistor and the second N-channel transistor (i.e., between the outputs of the level shifter circuit).

For claim 2, the medication above shows the resistance element (P5, Figure 8 of Nojiri) is constructed of a P-channel transistor (P5) having its gate grounded to be normally ON, and the P-channel transistor is connected between the drains of the first and second N-channel transistors.

For claim 7, Figure 11A of Uenishi et al. in the above modification shows the drain of the first N-channel transistor (Qn1) serves as a second output terminal (103), wherein the first and second output terminals are differential output terminals for the high power-supply voltage operating circuit.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uenishi et al. (USP 6,617,896) in view of Nojiri (US 2001/0013795 A1), as discussed in claim 1 above, and further in view of Shin et al. (USP 5,378,932).

With respect to claim 3, the modification of Uenishi et al. and Nojiri as discussed in claim 1 above all the limitations of this claim except for the resistance element comprising an N-channel transistor having its gate connected to a high voltage supply. However, Shin et al. teaches in Figure 12 a resistance element that is constructed of a NMOS transistor having its gate connected to a high supply voltage so that the NMOS transistor is normally ON. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the level shift circuit in the above modification (Uenishi et al. in view of Nojiri) by using the resistance element that is constructed of an N-channel transistor having its gate connected to a high supply voltage as taught in Figure 12 of Shin et al. since the circuitry would

have been functionally equivalent and that the circuit designer would have more flexibility in designing the circuitry depending on the availability of the materials when designing the circuitry. Thus, this medication/combination meets all the limitations of claim 3.

Allowable Subject Matter

Response to Arguments

7. Applicant's arguments with respect to the Shimazaki et al. reference have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments, with respect to the Wang et al. reference, filed on 12/14/09 have been fully considered but they are not persuasive.

Note that applicant argues that the transistor MN4 in Figure 3 of Wang controlled by the XNOR gate 264 to be in the OFF state during the operation of the level shifter, and thus the transistor MN4 of Wang does not serve as a resistor during the operation of the level shift circuit. However, this argument is not persuasive because the recitation "a resistor" during the operation of the level shift circuit is not recited in the claim. Note that the claim only requires a resistance element connected between the drains of the first and second N-channel transistors. Clearly, transistor MN4 is a resistance element connected between the first and second N-channel transistors MN2 and Mn3.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Long Nguyen/
Primary Examiner
Art Unit 2816